IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: **TOKUDA, Kazuhiko**

Group Art Unit: **3729**

Serial No.: 09/928,441

Examiner: **Rick Kiltae Chang**

Filed: **August 14, 2001**

P.T.O. Confirmation No.: **8352**

For: **A METHOD OF FORMING WIRING LINES ON A BOARD TO FORM A CIRCUIT BOARD**

Request for Reconsideration under 37 C.F.R. § 1.11

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 27, 2005

Sir:

This is a Request for Reconsideration under 37 C.F.R. § 1.11 filed in response to the Office Action dated April 8, 2005, which issued following a Notice of Appeal and filing of Appeal Brief in the above-identified Application.

In this application, only two claims are being prosecuted, Claims 37 and 38, as last amended on July 27, 2004. These two claims are as follows:

Claim 37 A method of forming a plurality of wiring lines on conductive material on a board having a core layer to form a printed circuit board, comprising:

(a) forming said plurality of wiring lines on a surface of said core layer, having first and second portions, the plurality of wiring lines formed on said surface of said core having side walls of a uniform thickness in height relative to said surface of said core layer; and

(b) etching the first portion of a first of said plurality of wiring lines, such that the first portion has a planar surface completely across said first portion, joining said side walls, and is thinner in height relative to said surface of said core layer than the second portion, such that cross-talk noise between adjacent two wiring lines is reduced.

Claim 38 The method as claimed in Claim 37, wherein a second of said plurality of said wiring lines is provided, spaced from said first wiring line of said plurality of wiring lines having said first and second portions, said second wiring line having third and fourth portions, and etching said second wiring line such that the third portion is thinner in height relative to said surface of said core layer than the fourth portion.

These two claims, and their predecessors have previously been rejected using various references. For example:

1. In Office Actions dated October 29, 2002 and February 11, 2003, the claims were rejected as anticipated by Takahashi et al. (U.S. 4,413,309);

2. In Office Actions dated August 8, 2003 and December 31, 2003, the claims were rejected as anticipated by Barber (U.S. 4,701,363);

3. In Office Actions dated April 23, 2004 and September 7, 2004, the claims were rejected as obvious in view of a combination of the Barber reference with Seo et al. (U.S. 5,757,069); and

4. Now, after filing of a Notice of Appeal and a Appeal Brief, the Examiner has seen fit to withdraw the previous rejection and to allege that these claims are anticipated in view of an entirely

new reference, Gali et al. (U.S. 3,781,596). If these claims are so clearly anticipated by Gali et al., why was the reference not cited earlier?

In any event, Gali et al. does not teach or suggest the present method of forming a plurality of wiring lines on conductive material on a board having a core layer to form a printed circuit board such that cross-talk noise between adjacent two wiring lines is reduced.

In the Office Action, the Examiner alleges that: "Gali discloses that in Fig. 10, 71 is etched to form a plurality of wiring lines (col. 9, lines 10-11) on a surface of a core layer 10, and further etching 71 using mask 74 to form a different thickness first portion 12 than a second portion 13 (Fig. 1a)." Reconsideration and removal of this completely new rejection is respectfully requested in view of the following remarks.

Even assuming that the description of the Gali et al. reference made by the Examiner in the Office Action is valid, such does not teach or suggest the present claimed method.

At most, Gali et al. describes generally a method of etching a portion of a wiring line. It does not even approach the specific features of Applicants claimed method, with the results achieved.

In Gali et al., where is one to find any suggestion that "the plurality of wiring lines formed on said surface of said core having side walls of uniform thickness in height relative to said surface of said core layer" (Claim 37, lines 4-6)?

In Gali et al., where is one to find any suggestion that the "first portion has a planar surface completely across said first portion, joining said side wall" (Claim 37, lines 8-9)?

In Gali et al., where is there any suggestion that by carrying out the specific method steps of Applicant, "cross-talk noise between adjacent two wiring lines is reduced" (Claim 37, lines 10-11)?

Applicant requests that the Examiner, if this rejection is maintained, point out in the Gali et al. reference where the above specific features of Applicants Claim 37 are described or even hinted at. Certainly, one cannot refer to drawing figures, which all know are not drawn to scale.

It appears that, following a reading of Applicant's specification, the Examiner made an early decision that Claim 37 should not be allowed, for whatever reason, and has searched for various references, over almost a three year period, to justify that decision.

Unless the Examiner can point out in the Gali et al. reference how the specific features of Applicant's claims are anticipated, the rejection should be reconsidered and removed and Claims 37 and 38 allowed.

In the event that any fees are due in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

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